IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT	:	Yang et al.
SERIAL NO.	:	10/725,933
FILED	:	December 3, 2003
FOR	:	FAN OUT TYPE WAFER LEVEL PACKAGE STRUCTURE AND METHOD OF THE SAME
CONFIRMATION NO.	:	4487
EXAMINER	:	David A. Zarneke
ART UNIT	:	2891
ATTORNEY DOCKET NO.	:	HK9225US

DECLARATION UNDER 37 C.F.R. 1.132

1. The undersigned, **Wen-Kun Yang**, is a co-inventor of the above-identified U.S. Patent Application No. 10/725,933 (hereinafter referred to as the "'933 application").

2. The undersigned has 25 years of experience in the semiconductor manufacturing industry.

3. The undersigned is familiar with U.S. Patent No. 6,417,025 to Gengel (hereinafter "Gengel").

4. Gengel discloses an integrated circuit device package that includes a first dielectric layer 404 formed of silicon dioxide (SiO_2) or polymers (e.g., polyethersulfone (PES) or polysulfone (PS)); a functional component (die) 210; and a thermally conductive layer (base) 406.

5. The present invention has a "buffer layer" that includes **silicone rubber**, epoxy, resin or BCB (Benzocyclobutene).

6. Gengel's dielectric layer 404 cannot function as the applicant's "buffer layer" to release stress due to: (1) the properties (i.e., tensile strength, Young's modulus, glass transition temperature, stress index, and coefficient of thermal expansion(CTE)) of the materials used for dielectric layer 404; (2) the physical arrangement of dielectric layer 404 and functional component (die) 210; and (3) the lack of an adhesion material on Gengel's thermally conductive layer (base) 406.

7. The properties of **silicone rubber**, epoxy, resin and BCB, used for the applicant's buffer layer, are significantly different from the properties of **silicon dioxide (SiO_2)** and polymers (e.g., **polyethersulfone (PES) or polysulfone (PS)**), used by Gengel for dielectric layer 404.

8. **Silicone rubber** type materials has been used for this application and are not equivalent dielectric materials to Gengel's silicon dioxide (SiO_2) and polymers (e.g., PES or PS) due to the significant differences in their material properties, as indicated in the table below:

Items	Silicone Rubber	SiO_2	PES	PS
Tensile Strength	9.4MPa	96-386MPa	107MPa	76MPa
Young's Modulus	**<20MPa**	**69GPa**	**7.56GPa**	**4.87GPa**
Glass Transition Temp.	-60c	N/A	221c	225c
Stress Index	**0.84**		**54.8**	**54.5**
Elongation at break	130%		9.35%	24.8%
CTE	~200	0.6	37	56ppm/c

9. A temperature increase will induce stress in Gengel's package because (1) a lack of adhesion material between Gengel's dielectric layer 404 and thermally conductive layer (base) 406 and (2) the type of materials selected for Gengel's dielectric layer 404 (i.e., the CTE of

dielectric layer 404 is significantly higher than the CTE of functional component (die) 210). The induced stress will result in functional component (die) 210 being "squeezed" upward by dielectric layer 404 as it expands. Moreover, due to the shape of functional component (die) 210, it will be pushed away (i.e., displaced) from thermally conductive layer (base) 406.

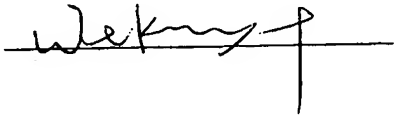
10. The present invention solves the stress induced problems of Gengel by providing a buffer layer comprised of **silicone rubber**, epoxy, resin or BCB (Benzocyclobutene).

11. Gengel's dielectric layer 404 functions only as a dielectric, not as a buffer layer.

12. The Applicant has proved that the Gengel's structure can not function the feature of the present invention. Please refer to the attachment one which is testing data prepared by the Advanced packing reach center, National Tsing Hua University. Please refer to the page 5-6, it indicates that the prior art structure suffers stress 55.3 MPa. Under the finite analysis, the chip of the prior art will be pushed up and cause the package failure. .

Note: The undersigned (Wen-Kun Yang) has been used the **Silicone rubber** types materials (Shin-Etsu Chemical Co. Ltd. Model number – X-35-259-21 and 21H) to develop and approval the invention. **But** do not use the other type materials for instant Epoxy, Resin, BCB to approve it due to the best materials is silicone rubber type materials for this invention.

The undersigned declarant is hereby warned that willful false statements and the like are punishable by fine or imprisonment, or both (18 U.S.C. 1001) and may jeopardize the validity of the application or any patent issuing thereon. All statements made of the declarant's own knowledge are true and all statements made on information and belief are believed to be true.

Date: Feb. 13, 2008 Signature: 

Name: **Wen-Kun Yang**

ACET/NTHU Project

The Reliability Analysis of Novel Slide-able Cu Trace Wafer Level Chip Scale Package - III

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http://csml9.pme.nthu.edu.tw:8080/csml/index.htm

Material Properties

Material	Young's Modulus (GPa)	Poisson Ratio	CTE (ppm/℃)
Chip Carrier, Alloy42	148	0.3	5
Adhesive, X35	0.05	0.4	167
Chip	129	0.28	2.62
Dielectric layer, 3170	0.09	0.41	150
Silicone rubber (w/Filler) , X35	0.05	0.4	167
Solder Mask	3.5	0.35	30
Photoresist, PI [1]	2.5	0.34	45
Polyethersulfone (PES) [2]	2.5	0.4	55

[1] http://www.goodfellow.com/csp/active/static/A/Polyimide.HTML

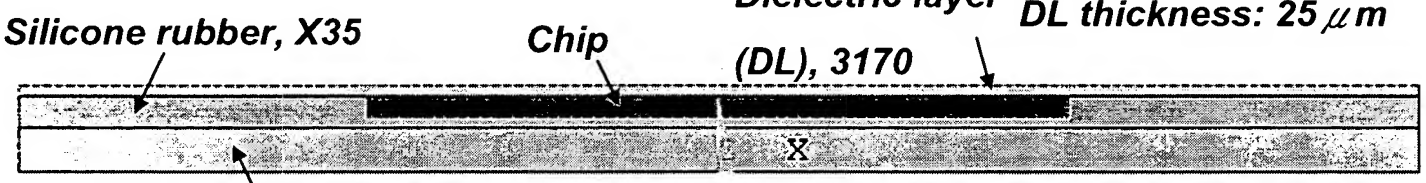
[2] http://www.goodfellow.com/csp/active/static/A/Polyethersulfone.HTML

Finite Element Analysis

- **Application structure**

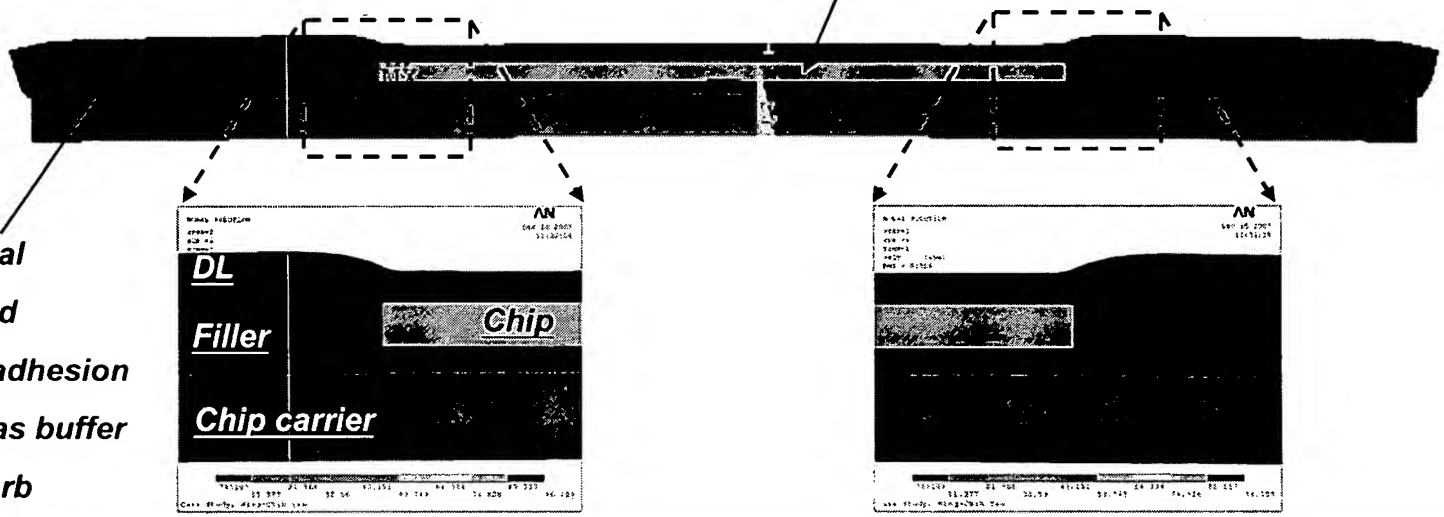
Chip size: 2mm
Package size: 4mm

Chip thickness: 50 μm
Adhesive thickness: 20 μm
Carrier thickness: 100 μm
DL thickness: 25 μm



From room temp. (25℃) to 125℃

Max. von Mises stress = 45.0 MPa



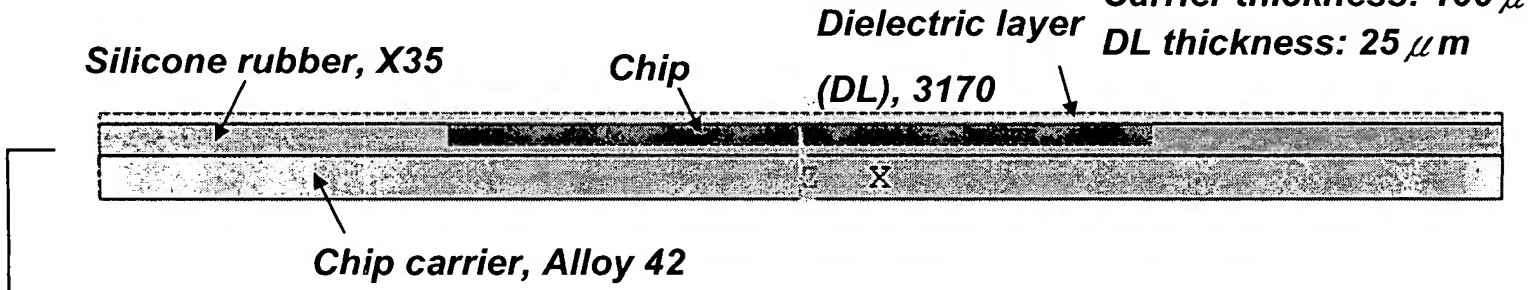
Due to material Properties and Structure (w/adhesion Layer), it act as buffer Layer to absorb The stress.

Finite Element Analysis

- **Application structure**

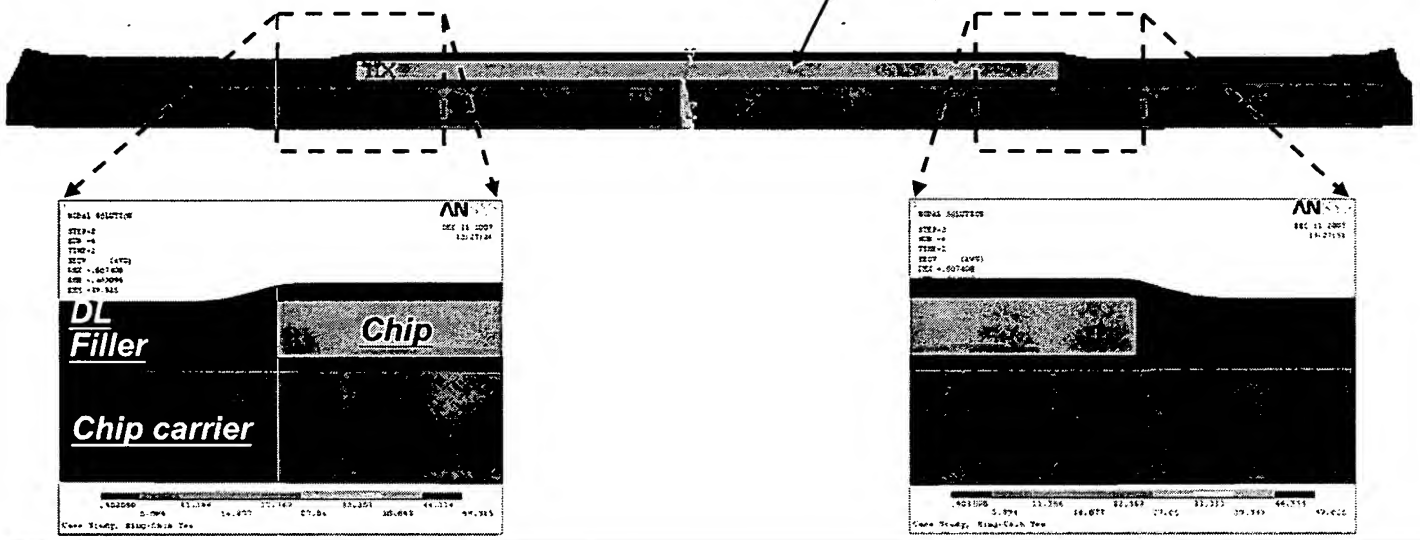
Chip size: 2mm
Package size: 4mm

Chip thickness: 50 μm
Adhesive thickness: 20 μm
Carrier thickness: 100 μm
DL thickness: 25 μm



From room temp. (25℃) to -40℃

Max. von Mises stress = 23.4 MPa

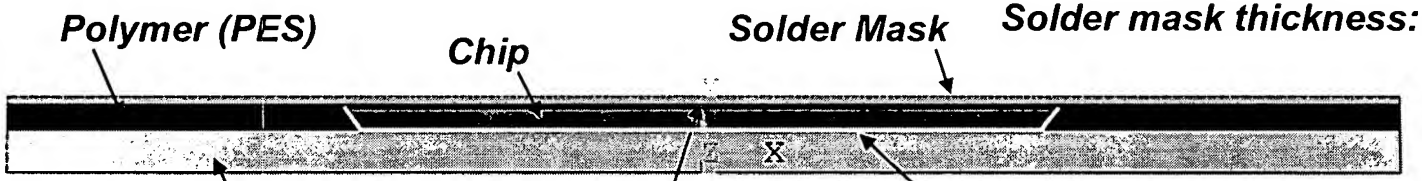


Finite Element Analysis

- **Structure of prior art**

Chip size: 2mm
Package size: 4mm

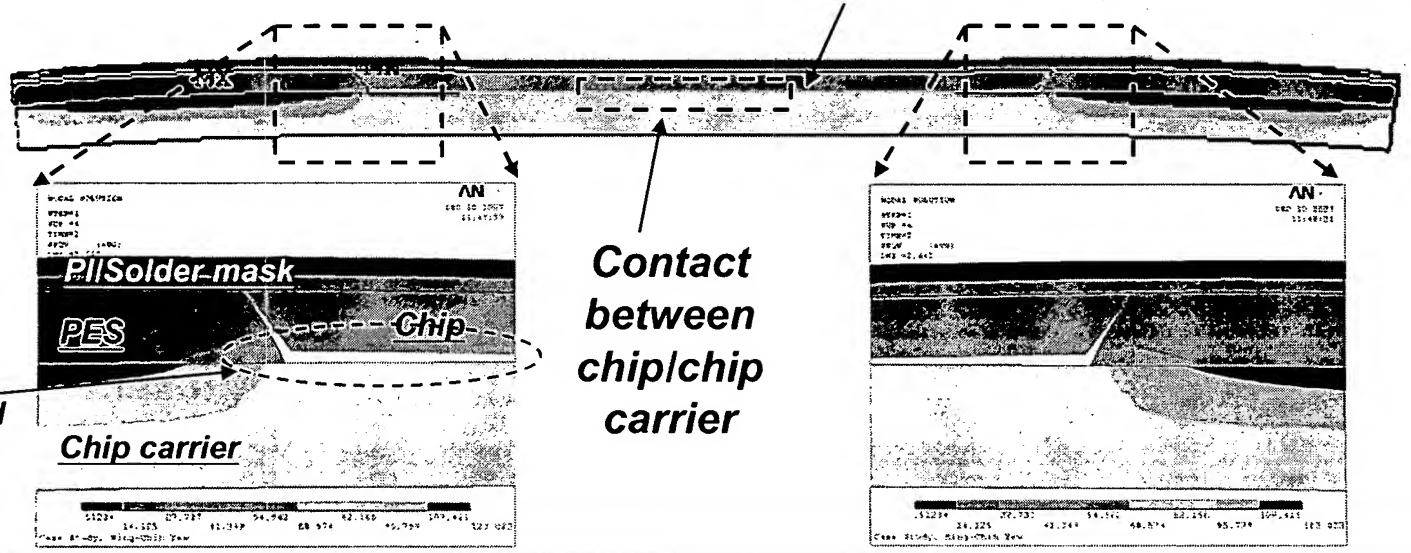
Chip thickness: 50 μm
Carrier thickness: 100 μm
PI thickness: 10 μm
Solder mask thickness: 15 μm



No adhesion, three contact pairs are established

From room temp. (25℃) to 125℃

Max. von Mises stress = 55.3 MPa



Contact between chip/chip carrier

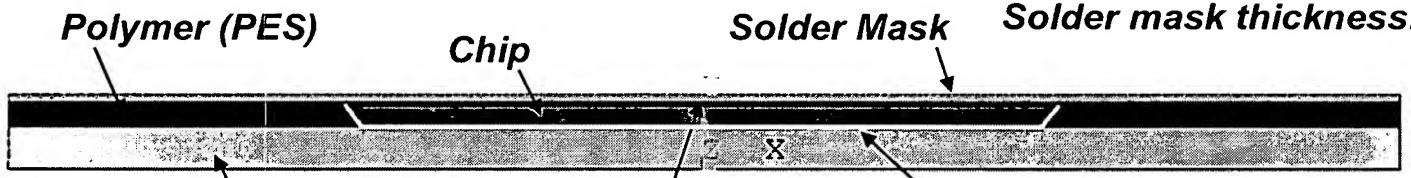
Chip be pushed To upside, gap Happen, stress happen

Finite Element Analysis

- **Structure of prior art**

Chip size: 2mm
Package size: 4mm

Chip thickness: 50 μm
Carrier thickness: 100 μm
PI thickness: 10 μm
Solder mask thickness: 15 μm



No adhesion, three contact pairs are established

From room temp. (25℃) to -40℃

Max. von Mises stress = 37.7 MPa